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Publication number: **0 670 602 A1**

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## EUROPEAN PATENT APPLICATION

21 Application number: **95102798.6**

51 Int. Cl.<sup>6</sup>: **H01L 27/06**

22 Date of filing: **27.02.95**

30 Priority: **28.02.94 JP 30672/94**

43 Date of publication of application:  
**06.09.95 Bulletin 95/36**

84 Designated Contracting States:  
**DE FR GB**

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54 **Field effect transistor having capacitor between source and drain electrodes.**

57 A semiconductor device having a field-effect transistor has a MOS capacitor formed on a principal surface of a semiconductor substrate of the semiconductor device, and connecting a first and a second electrodes of the MOS capacitor to a source electrode and a drain electrode, respectively, of the field-effect transistor.

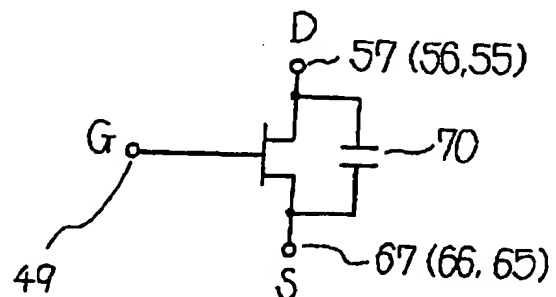


FIG. 3

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## BACKGROUND OF THE INVENTION

### Field of the Invention

The present invention relates to a semiconductor device having a junction type field-effect transistor (referred to as a junction type FET hereinafter).

### Description of the Prior Art

A plan view of a prior art semiconductor device having a conventional junction type FET is shown in FIG. 6(A), and an example of its circuit diagram is shown in FIG. 6(B).

Referring to FIG. 6(A), a source electrode (S) 2 and a drain electrode (D) 3 are formed on a surface of a semiconductor substrate (a semiconductor chip), where the electrodes 2 and 3 are composed respectively of bonding pads 21 and 23, and pluralities of finger parts 22 and 24 which extend respectively from the bonding pads 21 and 23 to the section above an N-type active region to be connected respectively to N<sup>+</sup>-type diffused layers formed in that section. Further, P<sup>+</sup>-type diffused layers are formed as a gate region (G) between the N<sup>+</sup>-type diffused layers, and a gate electrode is led out from a P<sup>+</sup>-type rear surface of the semiconductor substrate.

In the semiconductor device having the conventional junction type FET, a diode (Di) is formed between the gate electrode (G) and the source electrode (S) on the input side, and a Zener diode (Z-Di), for protecting the junction type FET against an overvoltage which is applied to the drain electrode, is formed between the drain electrode (D) and the source electrode (S) on the output side, as shown in FIG. 6(B) though omitted from FIG. 6(A). Such a technique is disclosed in, for example, Japanese Utility Model Application Laid-Open No. Hei 2-56438 (1990).

Since, however, the capacity (output capacity) between the source electrode and the drain electrode of the conventional junction type FET is a small parasitic capacity of the order of 2 to 3 pF, it is difficult to satisfactorily isolate high frequency noises from the outside. Because, this capacity is computed by  $C_{GD}$  (parasitic capacity between the gate electrode and the drain electrode) +  $C_{DS}$  - (parasitic capacity between the drain electrode and the source electrode). Since one has  $C_{DS} \approx 0$ , to obtain a large value for the capacity it is necessary to make  $C_{GD}$  large by increasing the area of the gate region of the P<sup>+</sup>-type diffused layer. However, an increase in the area of the gate region results in the deterioration in the characteristics, for example, a value of the conductance  $g_m$  of the junction type FET is decreasing.

On the other hand, obtaining a sufficiently large capacity between the source electrode and the drain electrode by means of the Zener diode for the protective circuit requires a very large area, which is unrealistic.

Moreover, since these capacities are P-N junction capacities, a magnitude of the capacity depends on the difference between potentials applied to the source electrode and the drain electrode so that an isolation performance against the high frequency noises from external circuits varies with the output level of the junction type FET.

Additionally, it is not possible to effectively isolate the high frequency noises even if a capacitive element is installed outside the semiconductor substrate (semiconductor chip) because the capacitive element connected between the source electrode and drain electrode is not provide nearby the junction type FET.

As described in the above, in the conventional junction type FET it is not possible to insulate noises from external circuits so that there is a problem in that the characteristics (mutual conductance and the like) of the junction type FET is not stabilizing.

In particular, when the junction type FET is incorporated in an electret capacitor microphone (miniaturized microphone used in a portable telephone set such as a land mobile radio telephone set or in a portable radio equipment) as an amplifier, there arises a problem that it is liable to pick up noises of frequency higher than 10 kHz under an influence of a high frequency oscillator which generates a carrier wave nearby the junction type FET.

On the other hand, in the electret capacitor microphone or the like, it is necessary to discharge the electric charge, charged between electrodes, quickly so that the adoption of the junction type FET having an input gate of diode construction is required and it is not possible to adopt a MOSFET having a large input capacity, namely, having an input gate of capacitor construction, because of the deterioration of a speed corresponding to an input signal.

### SUMMARY OF THE INVENTION

It is therefore an object of this invention to provide a semiconductor device which can effectively isolate noises impressed on the output side of the junction type FET.

It is another object of this invention to provide a semiconductor device which can effectively isolate input of the high frequency noises to the junction type FET without giving rise to an inconvenience to the intrinsic characteristics of the junction type FET.

It is still another object of this invention to provide a semiconductor device having the junction type FET suitable for use in an electret capacitor microphone.

It is a feature of this invention, in a semiconductor device having the junction type FET provided with a source electrode and a drain electrode on a principal surface of a semiconductor substrate, to form a MOS capacitor on the principal surface, and connect an upper electrode of the MOS capacitor to the source electrode and connect its lower electrode to the drain electrode. Here, the lower electrode may be constituted of a polysilicon film highly doped with an impurity such as boron or phosphorus, whereas the upper electrode may be constituted of a metallic film of aluminum or the like. In that case, it is preferable that the polysilicon film which is connected to the source or the drain electrode constituted the lower electrode by extending it on an insulating film formed on the principal surface to the region of formation of the MOS capacitor, and the drain or the source electrode and the upper electrode are formed integrally. Further, it is preferable that a capacitor dielectric film between the upper and the lower electrodes is constituted of a silicon oxide film, silicon nitride film, alumina film, phosphate glass film, borosilicate glass film, or a composite film formed by combining some of these films.

It is another feature of this invention, in a semiconductor device having an N-channel junction type FET which is provided with a source electrode and a drain electrode on a principal surface of a semiconductor substrate and has a P-type impurity region as a gate electrode, to form a MOS capacitor on the principal surface, connect an upper electrode of the MOS capacitor to the source electrode and connect its lower electrode to the drain electrode, and form on the semiconductor substrate a diode whose cathode is connected to the gate region and whose anode is connected to the source electrode. Here, a resistive element is formed on the semiconductor substrate, where one of the end parts of the resistive element may be connected to the source electrode and the other end part may be connected to the gate region.

It is another feature of this invention to form a source electrode and a drain electrode of a junction type FET on a principal surface of a semiconductor substrate, connect a MOS capacitor formed on the principal surface between the source electrode and the drain electrode, and use the device by incorporating it in an electret capacitor microphone.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The above-mentioned and other objects, features and advantages of this invention will become

more apparent by reference to the following detailed description of the invention taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a plan view showing the semiconductor device (semiconductor chip) of a first embodiment according to the invention;

FIG. 2 shows sectional views of the first embodiment of the semiconductor device according to the invention, where FIGS. 2(A), 2(B), 2(C) and 2(D) show the A-A' part, B-B' part; C-C' part and D-D' parts, respectively, of FIG. 1;

FIG. 3 is an equivalent circuit diagram showing the first embodiment of the semiconductor device according to the invention;

FIG. 4 is a schematic diagram showing the case of incorporating the embodiment of the semiconductor device according to the invention;

FIG. 5 shows a second embodiment of the semiconductor device (semiconductor chip) of the invention, where FIG. 5(A) is a plan view, FIGS. 5(B) and 5(C) are sectional views of B-B' part and C-C' part, respectively of FIG. 5(A); and FIG. 6 is a diagram showing a prior art semiconductor device, where FIGS. 6(A) and 6(B) are a plan view and an equivalent circuit diagram.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to the drawings, this invention will be described in the following.

FIG. 1 shows a semiconductor chip 50 having the first embodiment of the junction type FET has a junction type FET 60 and a MOS capacitor 70.

A 4  $\mu\text{m}$ -thick N-type silicon epitaxial layer 61 is formed on a P<sup>+</sup>-type silicon substrate 11, and a P<sup>+</sup>-type element isolation region 12 is formed extending from a principal face (surface) 13 reaching the P<sup>+</sup>-type silicon substrate 11, constituting a semiconductor substrate.

FIG. 2(D) shows 2  $\mu\text{m}$ -deep slender N<sup>+</sup>-type source regions 62 and N<sup>+</sup>-type drain regions 63 extending in the X direction in FIG. 1. FIG. 2(A) shows slender 1.5  $\mu\text{m}$ -wide and 3  $\mu\text{m}$ -deep P<sup>+</sup>-type gate regions 64 that extend in the same manner are formed between the two kinds of regions within the islandlike N-type silicon epitaxial layer 61. The N<sup>+</sup>-type source region 62, the N<sup>+</sup>-type drain region 63 and P<sup>+</sup>-type gate region 64 are alternately arrayed, in the Y direction in FIG. 1. The P<sup>+</sup>-type gate regions 64 are connected at their end parts to the P<sup>+</sup>-type element isolation region 12, and are connected to a gate electrode 49 formed on the rear face of the P<sup>+</sup>-type silicon substrate.

A 1  $\mu\text{m}$ -thick silicon oxide film 14 is formed on the principal face 13, contact holes 16 reaching the respective source and the drain regions 63 and 63

are formed, and a 500 nm-thick silicon nitride film 15 is formed covering the top face of the silicon oxide film 14 and the side surfaces of the contact holes 16.

An aluminum based metallic source electrode 67 (S) is formed on the silicon nitride film 15, where the source electrode 67 has a circular bonding pad 66 and rectangular finger parts 65. The rectangular finger parts 65 are connected ohmically to the respective N<sup>+</sup>-type source regions 62 through the contact holes 16. Similarly, an aluminum based metallic drain electrode 57 (D) is formed on the silicon nitride film 15, where the drain electrode 57 has a circular bonding pad 56 and rectangular finger parts 55. The rectangular finger parts 55 are connected ohmically to the respective N<sup>+</sup>-type drain regions 63 through the contact holes 16.

FIG. 2(B) shows a MOS capacitor 70 formed on the silicon oxide film 14 on the out side of the islandlike N-type silicon epitaxial layer 61. The MOS capacitor 70 is constituted of a lower electrode 71 made of 1 μm-thick polysilicon film which contains an impurity such as phosphorus or boron at a high concentration of more than  $1 \times 10^{18} \text{ cm}^{-3}$  to reduce the electrical resistance formed on the silicon oxide film 14, a dielectric film 73 of silicon oxide formed on one part of the lower electrode 71, and an upper electrode made of an aluminum based metal which is formed on the dielectric film 73 via an opening 17 in the silicon nitride film 15.

FIG. 2(C) shows the lower electrode 71 connected to the bonding pad 56 of the drain electrode 57 via a connecting part 48 formed extending on the silicon oxide film 14 and a contact hole 18 formed in the silicon nitride film 15.

On the other hand, the upper electrode 72 is connected to the bonding pad 66 of the source electrode 67 via an aluminum based connecting part 47 extending on the silicon nitride film 15. The bonding pad 66 of the source electrode 67 and the finger parts 65, and the connecting part 47 and the upper electrode 72 of the MOS capacitor 70 are formed integrally using an aluminum based metal.

When the thickness of the dielectric film 73 of silicon oxide is 50 nm, and the area of the capacitor, namely, the shape of the opening 17 where the upper electrode 72 makes contact with the dielectric film 73, is a square of a side of 170 μm, the capacitance value of the MOS capacitor 70 turns out to be 20 pF.

By inserting such a MOS capacitor 70 between the source electrode 67 and the drain electrode 57 the cut-off frequency  $f$  for the case where the input impedance of the circuit driven by the junction type FET is, for example, 1 MΩ, becomes  $f' = 1/(2\pi \times CR) = 1/\{2\pi \times 20(\text{pF}) \times 1 (\text{M}\Omega)\} = 8 \times 10^3 [\text{Hz}] = 8 [\text{kHz}]$ .

The MOS capacitor 70 connected between the source electrode 67 and the drain electrode 57 of the junction type FET has the function of a low pass filter which obstructs the passage of the frequency component (high frequency) higher than the cut-off frequency  $f'$ .

Although the case of 20 pF for the capacitance value of the MOS capacitor 70 and the load resistance value of 1 MΩ is described in the above, the capacitance value can freely be determined depending on the resistance value and the frequency desired to be cut off.

Figure 4 is a schematic diagram showing a part of an electret capacitor microphone which uses the semi-conductor device having the junction type FET of this invention.

The microphone uses a diaphragm (electret diaphragm) 91 made of a polymer film subjected to a special treatment so as to be imparted with the electret phenomenon in order to obviate the need for an external dc power supply. The back electrode 92 which faces the diaphragm 91 is connected to the gate electrode G of the junction type FET 60 of this invention in which a MOS capacitor 70 is connected between the source and the drain, and supplies an input electrical signal to the FET 60 based on a sound 100.

The positive side of a battery 93 is connected to the drain electrode D of the FET, and its negative side is connected to the source electrode S of the FET. Further, the source electrode S is grounded via an output resistance  $R_{OUT}$  94.

A diode ( $D_1$ ) 95 which converts a capacity component to an input voltage component is installed, and a diode ( $D_2$ ) 96, a resistive element (R) 98 and a diode ( $D_3$ ) 97 for quickly discharging the electric charges charged between the diaphragm system and the junction type FET are formed between the source electrode and the gate electrode of the junction type FET 60. Of these components the diode ( $D_3$ ) 97 is the parasitic capacity between the source electrode and the gate electrode of the junction type FET 60. The resistive element (R) 98 is provided in order to discharge the charged electric charge corresponding to a voltage of 0 to 0.5 V, since a diode is not actuated until a voltage of the order of 0.6 V is applied across its both ends.

In FIG. 4, the region surrounded by the chain line 50 corresponds to the semiconductor device of the first embodiment shown in FIG. 1 through FIG. 3. The junction type FET 60, the MOS capacitor 70 and the parasitic diode (diode formed by the P-N junction within the junction type FET) 97 are formed in the semiconductor device 50, and other elements are externally connected to various terminals (marked by small open circles on the chain line 50 in FIG. 4) of the semiconductor device.

On the other hand, the region indicated by the chain line 80 in FIG. 4 shows the semiconductor device 80 of a second embodiment in which the diode ( $D_2$ ) 96 and the resistive element (R) 98 are also integrated on the semiconductor chip.

In FIG. 5, the parts with functions identical or similar to those of FIG. 1 through FIG. 3 are marked with identical symbols to omit overlapped description.

In FIG. 5(A) and FIG. 5(B), a P-type impurity region 81 is formed within an islandlike N-type silicon epitaxial layer 61' surrounded by the P<sup>+</sup>-type element isolation region 12, and an N-type impurity region 82 is formed within the region 81. The diode ( $D_2$ ) 96 is constituted of the P-N junction between both regions 81 and 82. An aluminum based connecting part 83 extends on a silicon nitride film 19 from the bonding pad 66 of the source electrode 67, and is connected to the P-type impurity region 81 via a contact hole 85. An aluminum based connecting part 84 connected to the N-type impurity region 82 via a contact hole 86, is coupled with the gate region and the gate electrode by being connected to the P<sup>+</sup>-type element isolation region 12 via a contact hole 87. The diode ( $D_2$ ) 96 is connected in this manner between the source and the gate of the junction type FET 60.

In FIG. 5(C), the resistive element (R) 96 with breadth of 20  $\mu\text{m}$ , length of 200  $\mu\text{m}$  and thickness of 0.8  $\mu\text{m}$ , made of polycrystalline silicon with resistivity  $1 \times 10^9 \Omega \cdot \text{cm}$ , is formed on the silicon oxide film 14. One of the end parts of the resistive element (R) 98 is connected via a contact hole 89 to the connecting part 83 from the source electrode, and the other end part of the resistive element 98 is connected via a contact hole 88 to the P<sup>+</sup>-type element isolation region 12 to be coupled with the gate region and the gate electrode. The resistive element (R) 98 is connected in this manner between the source and the gate of the junction type FET 60.

In the above examples, a silicon oxide film with relative dielectric constant of 3.7 to 3.9 is used as the dielectric film 73. However, a silicon nitride film with relative dielectric constant 6.0 to 7.4, an alumina film, a phosphosilicate glass film or a borophosphosilicate glass film, or a composite dielectric film formed by combining these films can also be used as the dielectric film 73.

As has been described in the above, this invention has a MOS capacitor connected between the source and the drain of a junction type FET, so that it is possible to isolate noises from external circuits driven by the junction type FET. As a result, it is possible to suppress especially the fluctuations in the mutual conductance characteristic of the junction type FET.

Moreover, even when the junction type FET is incorporated in an electret capacitor microphone in which a high frequency oscillator is installed nearby, it is possible to effectively isolate the high frequency noises from the high frequency oscillator.

Although the invention has been described with reference to specific embodiments, this description is not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as other embodiments of the invention, will become apparent to persons skilled in the art upon reference to the description of the invention. It is therefore contemplated that the appended claims will cover any modifications or embodiments as fall within the true scope of the invention.

### Claims

1. A semiconductor device comprising:
  - a field-effect transistor having a source electrode and a drain electrode formed in a semiconductor substrate;
  - a capacitor connected between said source electrode and said drain electrode formed in said semiconductor substrate.
2. The semiconductor device as claimed in claim 1, wherein said field-effect transistor has a gate electrode for receiving a input signal.
3. The semiconductor device as claimed in claim 2, further comprising a diode element connected between said gate electrode and said source electrode for discharging an electric charge between said gate electrode and said source electrode.
4. The semiconductor device as claimed in claim 3, further comprising a resistor connected between said gate electrode and said source electrode.
5. A semiconductor device comprising a first layer of a first conductivity type, a second layer of a second conductivity type selectively formed in said first layer, a gate region of said first conductive type selectively formed in said second layer, said second layer thereby having a drain region, a source region and a channel region, a first insulating film covering said first and second layers and said gate region, a drain electrode formed on said first insulating film and having a portion connected to said drain region through a first opening formed in said first insulating film, a source electrode formed on said first insulating film and having a portion connected to said source region

through a second opening formed in said first insulating film, a lower electrode formed on said first insulating film and connected to one of said source and drain electrodes, a dielectric film formed on said lower electrode, and an upper electrode formed on said dielectric film and connecting to the other of said source and drain electrodes.

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6. The semiconductor device as claimed in claim 5, further comprising a resistive film formed on said first insulating film and connected to said source electrode.

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7. The device as claimed in claim 6, further comprises a PN diode formed in said first layer in isolation therefrom, said PN diode being connected between said source electrode and the gate region.

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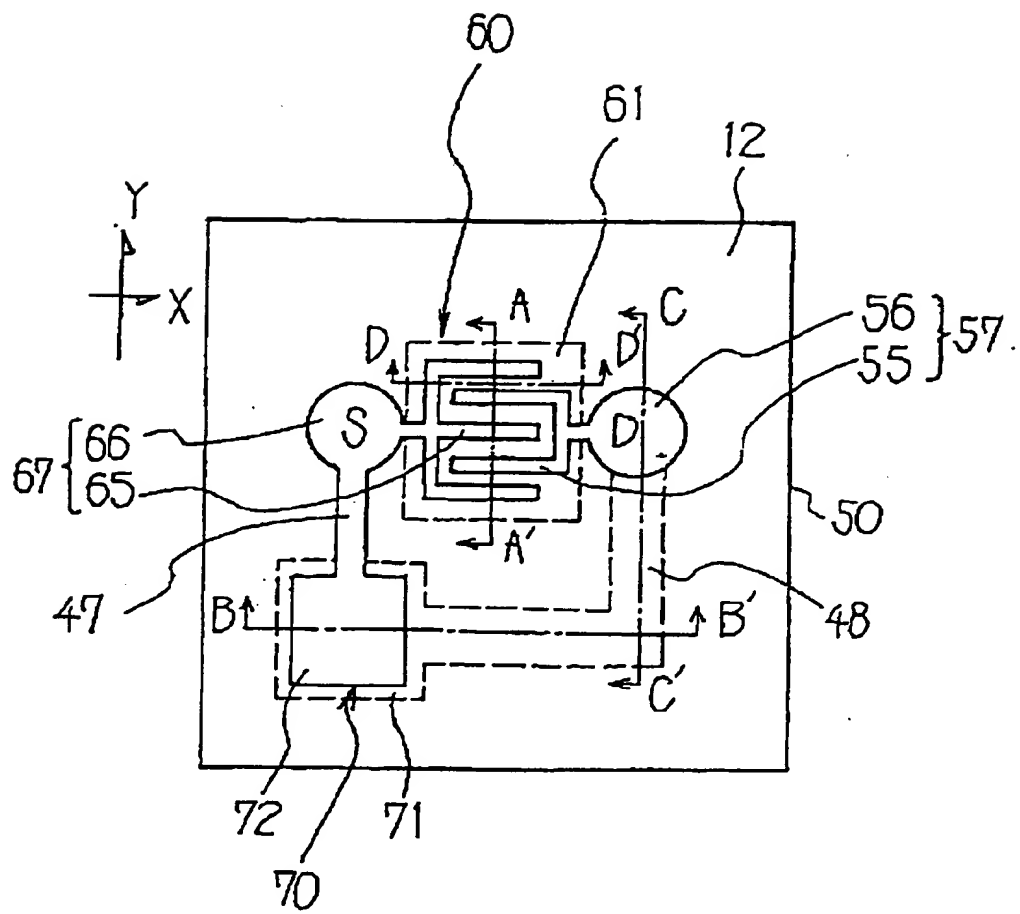
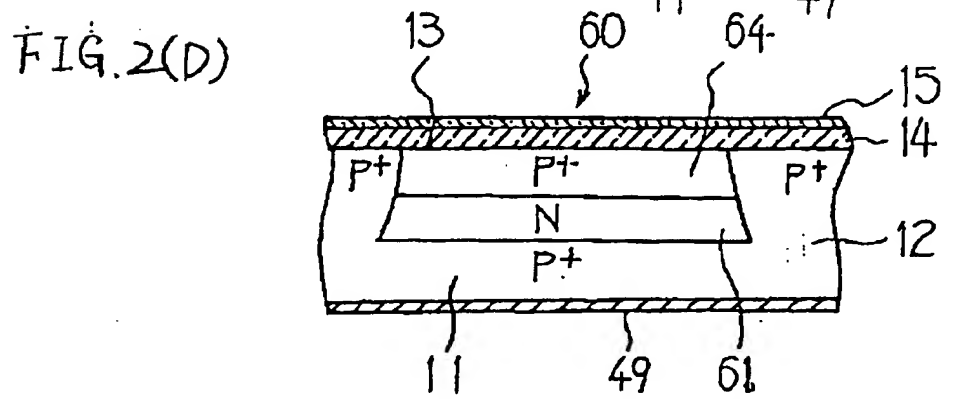
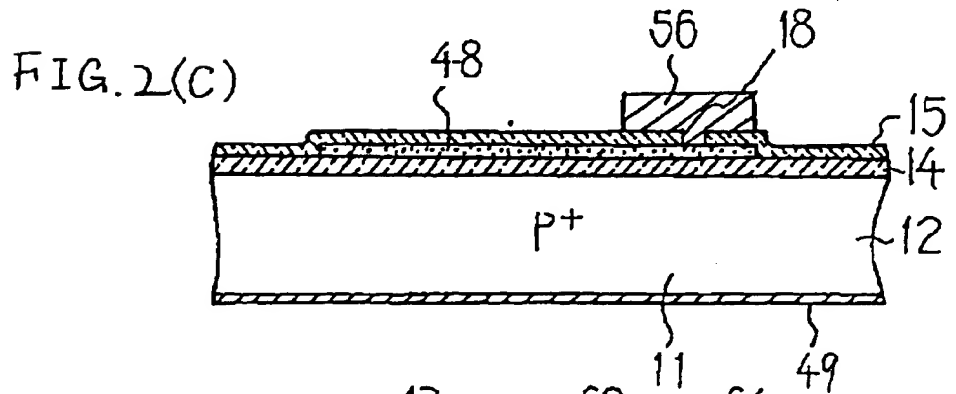
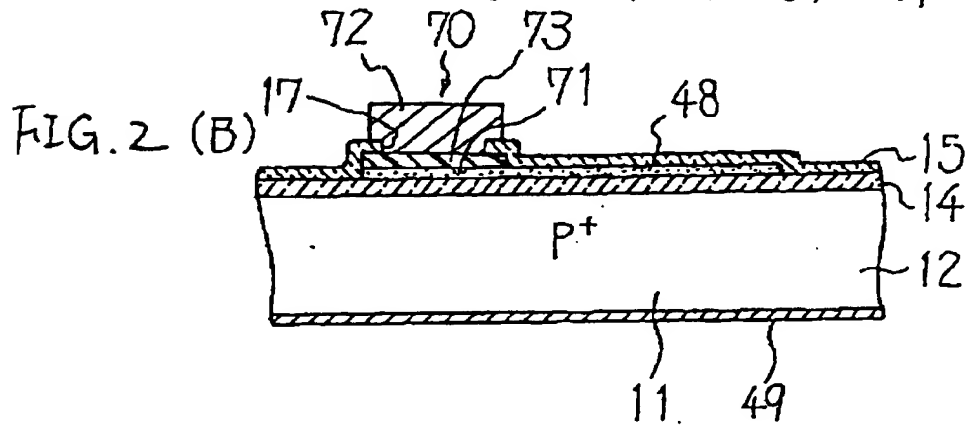
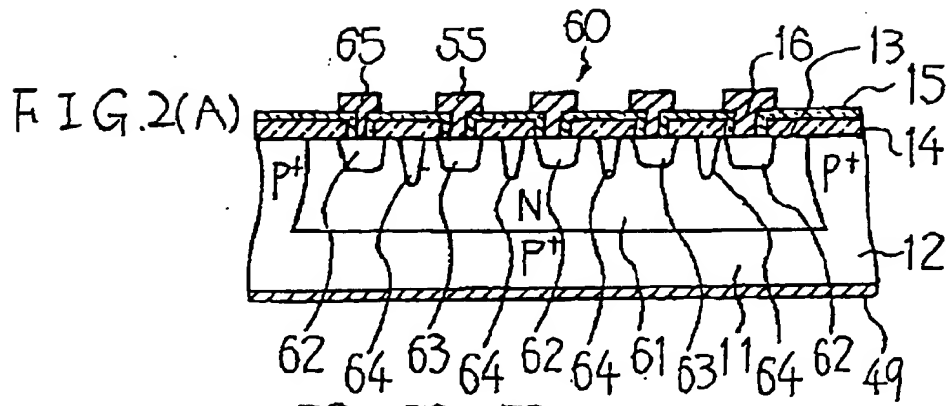


FIG. 1



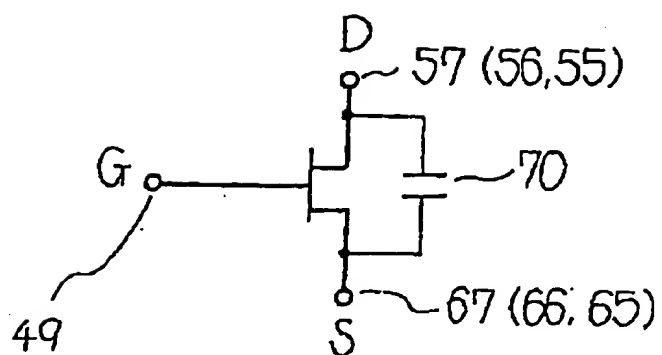


FIG. 3

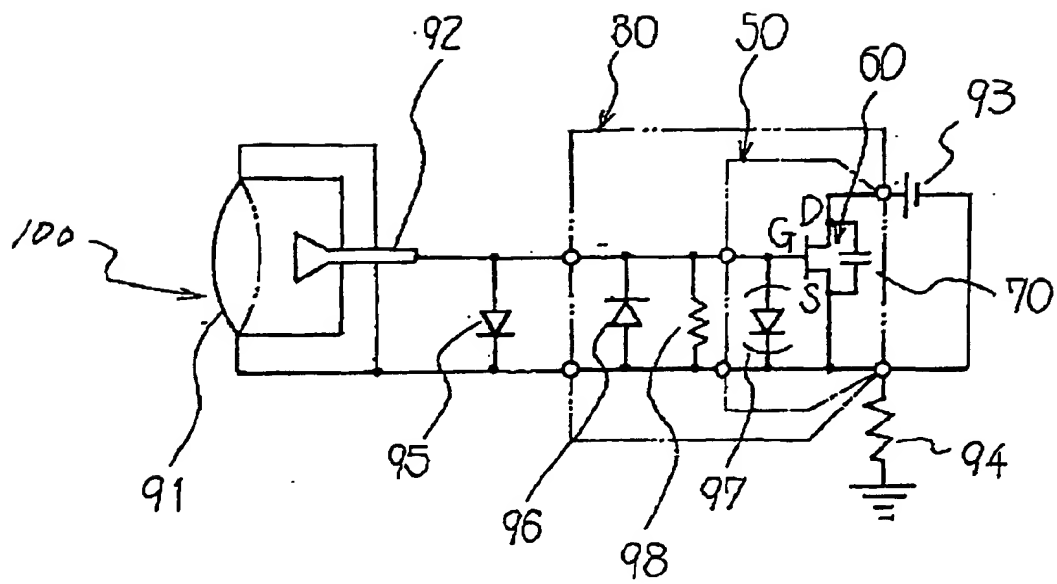


FIG. 4

FIG. 5(A)

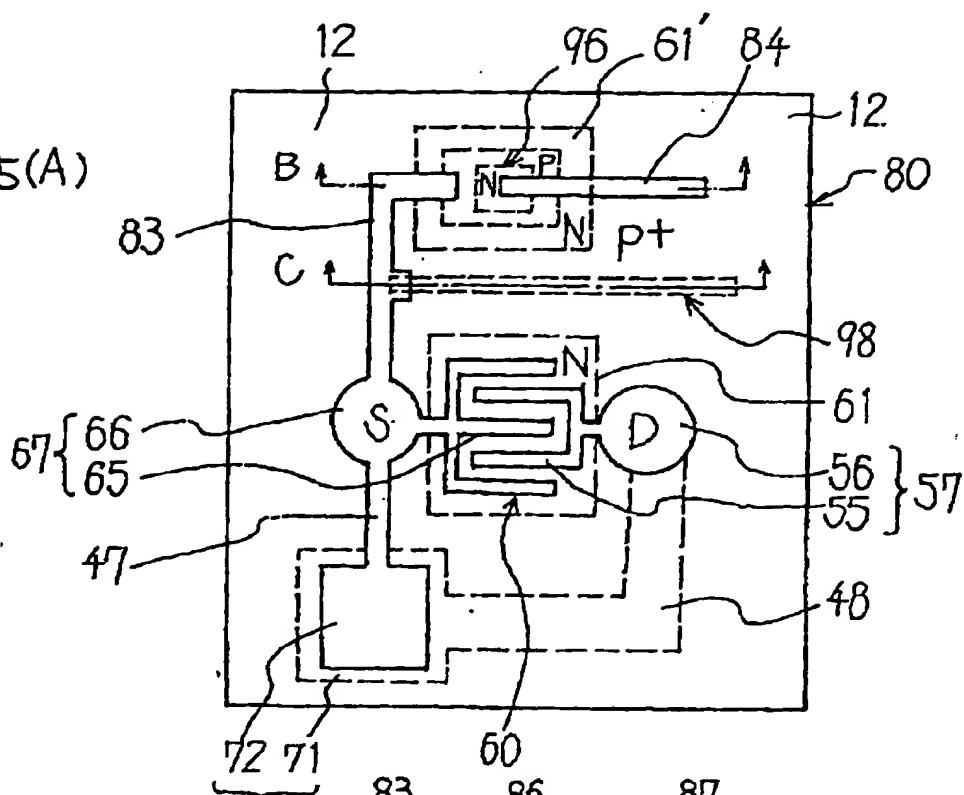


FIG. 5(B)

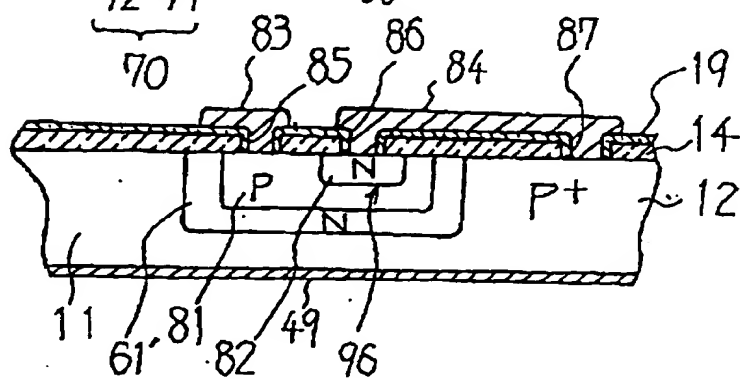


FIG. 5(C)

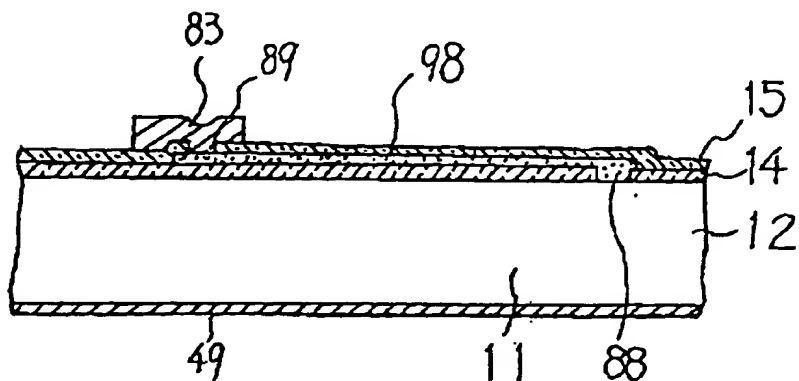


FIG. 6(A)  
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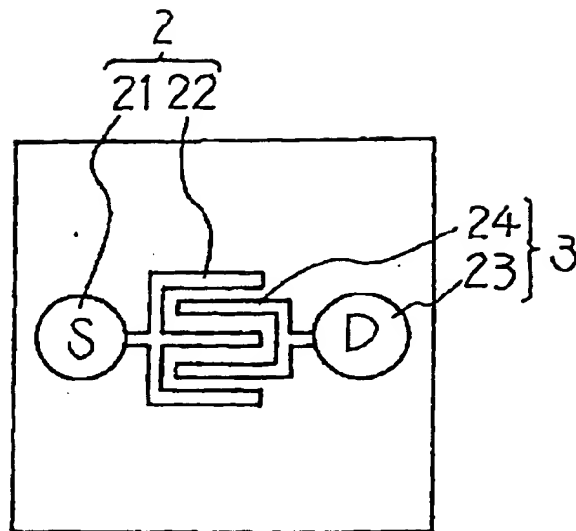
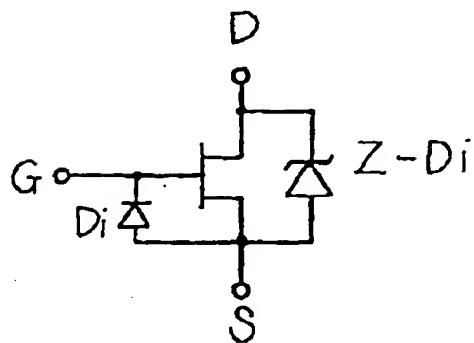


FIG. 6(B)  
PRIOR ART





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## EUROPEAN SEARCH REPORT

Application Number  
EP 95 10 2798

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	DE-A-40 24 728 (FUJI ELECTRIC CO LTD) 7 February 1991 * figures 10B, 20B * ---	1-4	H01L27/06
X	US-A-4 974 039 (SCHINDLER MANFRED J ET AL) 27 November 1990 * abstract; claims; figures * ---	1,2	
Y	US-A-3 492 511 (CRAWFORD ROBERT H) 27 January 1970 * column 4, line 19 - line 28; figure 6 * ---	1-7	
Y	PATENT ABSTRACTS OF JAPAN vol. 008 no. 259 (P-317) ,28 November 1984 & JP-A-59 129909 (SUWA SEIKOSHA KK) 26 July 1984, * abstract * ---	1-7	
A	PATENT ABSTRACTS OF JAPAN vol. 006 no. 211 (E-137) ,23 October 1982 & JP-A-57 114287 (TOKYO SHIBAURA DENKI KK) 16 July 1982, * abstract * ---	4,6	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
D,A	JP-U-02 056 438 (JFET) 1990 * the whole document * -----	3,7	H01L
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 15 June 1995	Examiner Vendange, P
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